	Document ID	U	Title	Current OR
179	US 5471591 A	☒	Combined write-operand queue and read-after-write dependency scoreboard	712/217
180	US 5465340 A	☒	Direct memory access controller handling exceptions during transferring multiple bytes in parallel	710/26
181	US 5461715 A	☒	Data processor capable of execution of plural instructions in parallel	712/212
182	US 5450555 A	☒	Register logging in pipelined computer using register log queue of register content changes and base queue of register log queue pointers for respective instructions	712/228
183	US 5448707 A	☒	Mechanism to protect data saved on a local register cache during inter-subsystem calls and returns	712/228
184	US 5430860 A	☒	Mechanism for efficiently releasing memory lock, after allowing completion of current atomic sequence	711/155
185	US 5430842 A	☒	Insertion of network data checksums by a network adapter	709/236
186	US 5430742 A	☒	Memory controller with ECC and data streaming control	714/764
187	US 5416907 A	☒	Method and apparatus for transferring data processing data transfer sizes	710/66
188	US 5392406 A	☒	DMA data path aligner and network adaptor utilizing same	710/316
189	US 5381538 A	☒	DMA controller including a FIFO register and a residual register for data buffering and having different operating modes	711/156
190	US 5376842 A	☒	Integrated circuit with reduced clock skew and divided power supply lines	326/21
191	US 5353332 A	☒	Method and system for stack memory alignment utilizing recursion	700/90
192	US 5333274 A	☒	Error detection and recovery in a DMA controller	714/50
193	US 5321821 A	☒	System for processing parameters in instructions of different format to execute the instructions using same microinstructions	712/210
194	US 5313644 A	☒	System having status update controller for determining which one of parallel operation results of execution units is allowed to set conditions of shared processor status word	712/228
195	US 5307506 A	☒	High bandwidth multiple computer bus apparatus	710/307
196	US 5301289 A	☒	Cache device for supplying a fixed word length of a variable instruction code and instruction fetch device	711/213
197	US 5300811 A	☒	Integrated circuit device and microprocessor constituted thereby	257/691
198	US 5278466 A	☒	Integrated circuit with reduced clock skew	326/95
199	US 5276684 A	☒	High performance I/O processor	370/438
200	US 5233698 A	☒	Method for operating data processors	713/601

	Document ID	U	Title	Current OR
156	US 5594863 A	☒	Method and apparatus for network file recovery	714/15
157	US 5590358 A	☒	Processor with word-aligned branch target in a byte-oriented instruction set	712/204
158	US 5590310 A	☒	Method and structure for data integrity in a multiple level cache system	711/146
159	US 5584009 A	☒	System and method of retiring store data from a write buffer	711/117
160	US 5574849 A	☒	Synchronized data transmission between elements of a processing system	714/12
161	US 5566312 A	☒	Processimg unit with programmable mis-aligned byte addressing	711/201
162	US 5566308 A	☒	Processor core which provides a linear extension of an addressable memory space	711/2
163	US 5566170 A	☒	Method and apparatus for accelerated packet forwarding	370/392
164	US 5557763 A	☒	System for handling load and/or store operations in a superscalar microprocessor	712/23
165	US 5551009 A	☒	Expandable high performance FIFO design which includes memory cells having respective cell multiplexors	711/165
166	US 5548786 A	☒	Dynamic bus sizing of DMA transfers	710/22
167	US 5544346 A	☒	System having a bus interface unit for overriding a normal arbitration scheme after a system resource device has already gained control of a bus	711/154
168	US 5535352 A	☒	Access hints for input/output address translation mechanisms	711/208
169	US 5533175 A	☒	Low cost page printer system and method	358/1.16
170	US 5519842 A	☒	Method and apparatus for performing unaligned little endian and big endian data accesses in a processing system	711/202
171	US 5519715 A	☒	Full-speed microprocessor testing employing boundary scan	714/727
172	US 5497476 A	☒	Scatter-gather in data processing system	711/112
173	US 5497468 A	☒	Data processor that utilizes full data width when processing a string operation	712/225
174	US 5497109 A	☒	Integrated circuit with reduced clock skew	326/93
175	US 5491802 A	☒	Network adapter for inserting pad bytes into packet link headers based on destination service access point fields for efficient memory transfer	709/236
176	US 5488730 A	☒	Register conflict scoreboard in pipelined computer using pipelined reference counts	712/41
177	US 5475852 A	☒	Microprocessor implementing single-step or sequential microcode execution while in test mode	714/34
178	US 5471598 A	☒	Data dependency detection and handling in a microprocessor with write buffer	711/122

	Document ID	U	Title	Current OR
135	US 5706465 A	☒	Computers having cache memory	711/123
136	US 5703579 A	☒	Decoder for compressed digital signals	341/50
137	US 5701517 A	☒	Pipelined alignment shifter and method for universal bit field boundary alignment	710/66
138	US 5689689 A	☒	Clock circuits for synchronized processor systems having clock generator circuit with a voltage control oscillator producing a clock signal synchronous with a master clock signal	709/400
139	US 5687314 A	☒	Method and apparatus for assisting data bus transfer protocol	714/49
140	US 5675807 A	☒	Interrupt message delivery identified by storage location of received interrupt data	710/260
141	US 5675579 A	☒	Method for verifying responses to messages using a barrier message	370/248
142	US 5671434 A	☒	Microprocessor controlled apparatus	712/38
143	US 5671413 A	☒	Method and apparatus for providing basic input/output services in a computer	713/2
144	US 5668984 A	☒	Variable stage load path and method of operation	712/222
145	US 5664162 A	☒	Graphics accelerator with dual memory controllers	345/532
146	US 5664150 A	☒	Computer system with a device for selectively blocking writebacks of data from a writeback cache to memory	711/143
147	US 5659782 A	☒	System and method for handling load and/or store operations in a superscalar microprocessor	712/23
148	US 5644729 A	☒	Bidirectional data buffer for a bus-to-bus interface unit in a computer system	710/310
149	US 5625787 A	☒	Superscalar instruction pipeline using alignment logic responsive to boundary identification logic for aligning and appending variable length instructions to instructions stored in cache	712/204
150	US 5625773 A	☒	Method of encoding and line breaking text	345/467
151	US 5615402 A	☒	Unified write buffer having information identifying whether the address belongs to a first write operand or a second write operand having an extra wide latch	712/38
152	US 5615349 A	☒	Data processing system capable of execution of plural instructions in parallel	712/212
153	US 5611064 A	☒	Virtual memory system	711/209
154	US 5608892 A	☒	Active cache for a microprocessor	711/118
155	US 5606670 A	☒	Method and apparatus for signalling a store buffer to output buffered store data for a load operation on an out-of-order execution computer system	711/154

	Document ID	U	Title	Current OR
112	US 5818834 A	☒	Serial bit rate converter embedded in a switching matrix	370/366
113	US 5813030 A	☒	Cache memory system with simultaneous access of cache and main memories	711/118
114	US 5812809 A	☒	Data processing system capable of execution of plural instructions in parallel	712/212
115	US 5812791 A	☒	Multiple sequence MPEG decoder	709/247
116	US 5812147 A	☒	Instruction methods for performing data formatting while moving data between memory and a vector register file	345/537
117	US 5809552 A	☒	Data processing system, memory access device and method including selecting the number of pipeline stages based on pipeline conditions	711/169
118	US 5790776 A	☒	Apparatus for detecting divergence between a pair of duplexed, synchronized processor elements	714/10
119	US 5787302 A	☒	Software for producing instructions in a compressed format for a VLIW processor	712/24
120	US 5774206 A	☒	Process for controlling an MPEG decoder	709/247
121	US 5761491 A	☒	Data processing system and method for storing and restoring a stack pointer	712/244
122	US 5761469 A	☒	Method and apparatus for optimizing signed and unsigned load processing in a pipelined processor	712/210
123	US 5758089 A	☒	Method and apparatus for burst transferring ATM packet header and data to a host computer system	709/234
124	US 5758051 A	☒	Method and apparatus for reordering memory operations in a processor	714/2
125	US 5754191 A	☒	Method and apparatus for optimizing pixel data write operations to a tile based frame buffer	345/563
126	US 5751955 A	☒	Method of synchronizing a pair of central processor units for duplex, lock-step operation by copying data into a corresponding locations of another memory	714/12
127	US 5751932 A	☒	Fail-fast, fail-functional, fault-tolerant multiprocessor system	714/12
128	US 5745723 A	☒	Data processing system capable of execution of plural instructions in parallel	712/212
129	US 5740398 A	☒	Program order sequencing of data in a microprocessor with write buffer	711/117
130	US 5732256 A	☒	CD-ROM optimization and stream splitting	707/1
131	US 5721957 A	☒	Method and system for storing data in cache and retrieving data from cache in a selected one of multiple data formats	710/66
132	US 5717946 A	☒	Data processor	712/225
133	US 5708843 A	☒	Method and apparatus for handling code segment violations in a computer system	712/23
134	US 5706483 A	☒	Run-time code compiler for data block transfer	345/562

	Document ID	U	Title	Current OR
90	US 5909559 A	☒	Bus bridge device including data bus of first width for a first processor, memory controller, arbiter circuit and second processor having a different second data width	710/307
91	US 5907860 A	☒	System and method of retiring store data from a write buffer	711/117
92	US 5887160 A	☒	Method and apparatus for communicating integer and floating point data over a shared data path in a single instruction pipeline processor	712/222
93	US 5887134 A	☒	System and method for preserving message order while employing both programmed I/O and DMA operations	709/200
94	US 5884269 A	☒	Lossless compression/decompression of digital audio data	704/501
95	US 5884231 A	☒	Processor apparatus and method for a process measurement signal	702/28
96	US 5878267 A	☒	Compressed instruction format for use in a VLIW processor and processor for processing such instructions	712/24
97	US 5878252 A	☒	Microprocessor configured to generate help instructions for performing data cache fills	712/225
98	US 5875466 A	☒	Active cache for a microprocessor	711/138
99	US 5867501 A	☒	Encoding for communicating data and commands	370/474
100	US 5862398 A	☒	Compiler generating swizzled instructions usable in a simplified cache layout	712/24
101	US 5860091 A	☒	Method and apparatus for efficient management of non-aligned I/O write request in high bandwidth raid applications	711/114
102	US 5859990 A	☒	System for transferring data segments from a first storage device to a second storage device using an alignment stage including even and odd temporary devices	710/33
103	US 5854914 A	☒	Mechanism to improved execution of misaligned loads	712/216
104	US 5852741 A	☒	VLIW processor which processes compressed instruction format	712/24
105	US 5841666 A	☒	Processor apparatus and method for a process measurement signal	702/189
106	US 5838894 A	☒	Logical, fail-functional, dual central processor units formed from three processor units	714/11
107	US 5835746 A	☒	Method and apparatus for fetching and issuing dual-word or multiple instructions in a data processing system	712/215
108	US 5832492 A	☒	Method of scheduling interrupts to the linked lists of transfer descriptors scheduled at intervals on a serial bus	707/101
109	US 5826054 A	☒	Compressed Instruction format for use in a VLIW processor	712/213
110	US 5819063 A	☒	Method and data processing system for emulating a program	703/27
111	US 5819058 A	☒	Instruction compression and decompression system and method for a processor	712/210

	Document ID	U	Title	Current OR
68	US 5983341 A	☒	Data processing system and method for extending the time for execution of an instruction	712/216
69	US 5982459 A	☒	Integrated multimedia communications processor and codec	348/425.3
70	US 5978899 A	☒	Apparatus and method for parallel processing and self-timed serial marking of variable length instructions	712/210
71	US 5977960 A	☒	Apparatus, systems and methods for controlling data overlay in multimedia data processing and display systems using mask techniques	345/563
72	US 5974104 A	☒	Data frame synchronizer for serial communication system	375/368
73	US 5973637 A	☒	Partial probe mapping	342/124
74	US 5966702 A	☒	Method and apparatus for pre-processing and packaging class files	707/1
75	US 5965514 A	☒	Microprocessor for supporting reduction of program codes in size	712/210
76	US 5964835 A	☒	Storage access validation to data messages using partial storage address data indexed entries containing permissible address range validation for message source	709/216
77	US 5951674 A	☒	Object-code compatible representation of very long instruction word programs	712/210
78	US 5949985 A	☒	Method and system for handling interrupts during emulation of a program	703/26
79	US 5949972 A	☒	System for memory error checking in an executable	714/54
80	US 5948096 A	☒	Apparatus and method for self-timed marking of variable length instructions having length-affecting prefix bytes	712/210
81	US 5941982 A	☒	Efficient self-timed marking of lengthy variable length instructions	712/210
82	US 5931944 A	☒	Branch instruction handling in a self-timed marking system	712/239
83	US 5926208 A	☒	Video compression and decompression arrangement having reconfigurable camera and low-bandwidth transmission capability	348/14.13
84	US 5924114 A	☒	Circular buffer with two different step sizes	711/110
85	US 5918005 A	☒	Apparatus region-based detection of interference among reordered memory operations in a processor	714/38
86	US 5915266 A	☒	Processor core which provides a linear extension of an addressable memory space	711/211
87	US 5914953 A	☒	Network message routing using routing table information and supplemental enable information for deadlock prevention	370/392
88	US 5913054 A	☒	Method and system for processing a multiple-register instruction that permit multiple data words to be written in a single processor cycle	712/220
89	US 5911152 A	☒	Computer system and method for storing data in a buffer which crosses page boundaries utilizing beginning and ending buffer pointers	711/208

	Document ID	U	Title	Current OR
45	US 6105119 A	☒	Data transfer circuitry, DSP wrapper circuitry and improved processor devices, methods and systems	711/219
46	US 6101568 A	☒	Bus interface unit having dual purpose transaction buffer	710/310
47	US 6084600 A	☒	Method and apparatus for high-speed block transfer of compressed and word-aligned bitmaps	345/545
48	US 6081570 A	☒	Parallel integrated frame synchronizer chip	375/368
49	US 6078280 A	☒	Periodic probe mapping	342/124
50	US 6070238 A	☒	Method and apparatus for detecting overlap condition between a storage instruction and previously executed storage reference instruction	712/217
51	US 6070010 A	☒	System and method of local data alignment for stack memory	717/154
52	US 6061687 A	☒	Linked lists of transfer descriptors scheduled at intervals	707/101
53	US 6058471 A	☒	Data processing system capable of executing groups of instructions in parallel	712/212
54	US 6055619 A	☒	Circuits, system, and methods for processing multiple data streams	712/36
55	US 6044448 A	☒	Processor having multiple datapath instances	712/9
56	US 6035426 A	☒	System for memory error checking in an executable	714/54
57	US 6026239 A	☒	Run-time code compiler for data block transfer	717/154
58	US 6021480 A	☒	Aligning a memory read request with a cache line boundary when the request is for data beginning at a location in the middle of the cache line	711/201
59	US 6021275 A	☒	Object code structure and method for translation of architecture independent program implementations	717/159
60	US 6016532 A	☒	Method for handling data cache misses using help instructions	711/118
61	US 6003122 A	☒	Direct memory access controller	711/201
62	US 5996057 A	☒	Data processing system and method of permutation with replication within a vector register file	712/5
63	US 5995122 A	☒	Method and apparatus for parallel conversion of color values from a single precision floating point format to an integer format	345/561
64	US 5991841 A	☒	Memory transactions on a low pin count bus	710/104
65	US 5991757 A	☒	Method and system for searching an array for an array value	707/3
66	US 5987593 A	☒	System and method for handling load and/or store operations in a superscalar microprocessor	712/206
67	US 5986677 A	☒	Accelerated graphics port read transaction merging	345/531

	Document ID	U	Title	Current OR
22	US 6247084 B1	☒	Integrated circuit with unified memory system and dual bus architecture	710/108
23	US 6247060 B1	☒	Passing a communication control block from host to a local device such that a message is processed on the device	709/238
24	US 6233702 B1	☒	Self-checked, lock step processor pairs	714/48
25	US 6230316 B1	☒	Patching rebased and realigned executable files	717/169
26	US 6230254 B1	☒	System and method for handling load and/or store operators in a superscalar microprocessor	712/23
27	US 6230215 B1	☒	On-demand transfer engine	710/1
28	US 6223268 B1	☒	System and method for writing specific bytes in a wide-word memory	711/201
29	US 6219773 B1	☒	System and method of retiring misaligned write operands from a write buffer	711/201
30	US 6219676 B1	☒	Methodology for cache coherency of web server data	707/201
31	US 6205536 B1	☒	Combined Instruction and address caching system using independent buses	712/38
32	US 6195741 B1	☒	Data processing device having a variable length code processing mechanism	712/24
33	US 6192461 B1	☒	Method and apparatus for facilitating multiple storage instruction completions in a superscalar processor during a single clock cycle	712/23
34	US 6191712 B1	☒	Circuit for aligning logical sectors with physical sectors in a disk storage system	341/95
35	US 6179489 B1	☒	Devices, methods, systems and software products for coordination of computer main microprocessor and second microprocessor coupled thereto	709/102
36	US 6175900 B1	☒	Hierarchical bitmap-based memory manager	711/156
37	US 6157967 A	☒	Method of data communication flow control in a data processing system using busy/ready commands	710/19
38	US 6151689 A	☒	Detecting and isolating errors occurring in data communication in a multiple processor system	714/49
39	US 6145017 A	☒	Data alignment system for a hardware accelerated command interpreter engine	710/5
40	US 6144322 A	☒	Variable length code processor with encoding and/or decoding	341/67
41	US 6131158 A	☒	Data processing system capable of executing groups of instructions, including at least one arithmetic instruction, in parallel	712/244
42	US 6131152 A	☒	Planar cache layout and instruction stream therefor	712/24
43	US 6119189 A	☒	Bus master transactions on a low pin count bus	710/110
44	US 6113650 A	☒	Compiler for optimization in generating instruction sequence and compiling method	717/160

	Document ID	U	Title	Current OR
1	US 20010030976 A1	☐	Packet conversion	
2	US 20010027496 A1	☒	Passing a communication control block to a local device such that a message is processed on the device	
3	US 20010023480 A1	☒	Conversion between packed floating point data and packed 32-bit integer data in different architectural registers	
4	US 20010023460 A1	☒	Passing a communication control block from host to a local device such that a message is processed on the device	
5	US 20010017089 A1	☒	Wallpaper manufacturing method, wallpaper manufacturing apparatus, and program for causing computer to function as wallpaper manufacturing apparatus	
6	US 20010016902 A1	☒	Conversion from packed floating point data to packed 8-bit integer data in different architectural registers	
7	US 20010016898 A1	☒	Data Processor	
8	US 6345357 B1	☒	Versatile branch-less sequence control of instruction stream containing step repeat loop block using executed instructions number counter	712/241
9	US 6341301 B1	☒	Exclusive multiple queue handling using a common processing algorithm	709/100
10	US 6334176 B1	☒	Method and apparatus for generating an alignment control vector	712/4
11	US 6334153 B1	☒	Passing a communication control block from host to a local device such that a message is processed on the device	709/230
12	US 6298370 B1	☒	Computer operating process allocating tasks between first and second processors at run time based upon current processor load	709/102
13	US 6292815 B1	☒	Data conversion between floating point packed format and integer scalar format	708/204
14	US 6289428 B1	☒	Superscaler processor and method for efficiently recovering from misaligned data addresses	711/201
15	US 6275504 B1	☒	Direct memory read and cell transmission apparatus for ATM cell segmentation system	370/471
16	US 6272499 B1	☒	Linked lists of transfer descriptors scheduled at intervals	707/102
17	US 6266769 B1	☒	Conversion between packed floating point data and packed 32-bit integer data in different architectural registers	712/221
18	US 6263426 B1	☒	Conversion from packed floating point data to packed 8-bit integer data in different architectural registers	712/229
19	US 6256715 B1	☒	System and method of performing gateway access	711/163
20	US 6253305 B1	☒	Microprocessor for supporting reduction of program codes in size	712/32
21	US 6247116 B1	☒	Conversion from packed floating point data to packed 16-bit integer data in different architectural registers	712/221

	Document ID	U	Title	Current OR
44	US 5561784 A	☒	Interleaved memory access system having variable-sized segments logical address spaces and means for dividing/mapping physical address into higher and lower order addresses	711/157
45	US 5550972 A	☒	Method and apparatus for efficient transfer of data to memory	345/537
46	US 5544337 A	☒	Vector processor having registers for control by vector resisters	712/4
47	US 5535345 A	☒	Method and apparatus for sequencing misaligned external bus transactions in which the order of completion of corresponding split transaction requests is guaranteed	710/305
48	US 5526510 A	☒	Method and apparatus for implementing a single clock cycle line replacement in a data cache unit	711/133
49	US 5473455 A	☒	Domain divided liquid crystal display device with particular pretilt angles and directions in each domain	349/124
50	US 5430884 A	☒	Scalar/vector processor	712/3
51	US 5386531 A	☒	Computer system accelerator for multi-word cross-boundary storage access	711/201
52	US 5335296 A	☒	Process for high speed rescaling of binary images	382/298
53	US 5291586 A	☒	Hardware implementation of complex data transfer instructions	712/220
54	US 5222225 A	☒	Apparatus for processing character string moves in a data processing system	710/22
55	US 5197130 A	☒	Cluster architecture for a highly parallel scalar/vector multiprocessor system	712/3
56	US 5095446 A	☒	Circuit for and method of controlling output buffer memory	345/571
57	US 4992956 A	☒	Apparatus for assembling data for supply to a scanning output device	358/1.15
58	US 4823286 A	☒	Pixel data path for high performance raster displays with all-point-addressable frame buffers	345/611
59	US 4777594 A	☒	Data processing apparatus and method employing instruction flow prediction	712/240
60	US 4750112 A	☒	Data processing apparatus and method employing instruction pipelining	712/217
61	US 4729119 A	☒	Apparatus and methods for processing data through a random access memory system	365/230.09
62	US 4654781 A	☒	Byte addressable memory for variable length instructions and data	711/219
63	US 4506345 A	☒	Data alignment circuit	377/54
64	US 4419701 A	☒	Data transducer position control system for rotating disk data storage equipment	360/77.08
65	US 4325120 A	☒	Data processing system	711/202

	Document ID	U	Title	Current OR
22	US 5790134 A	☒	Hardware architecture for image generation and manipulation	345/502
23	US 5778142 A	☒	Large capacity recording medium, method and apparatus for reproducing data from a large-capacity recording medium, and method and apparatus for recording data on a large-capacity recording medium	386/97
24	US 5752062 A	☒	Method and system for performance monitoring through monitoring an order of processor events during execution in a processing system	714/37
25	US 5751945 A	☒	Method and system for performance monitoring stalls to identify pipeline bottlenecks and stalls in a processing system	714/47
26	US 5748855 A	☒	Method and system for performance monitoring of misaligned memory accesses in a processing system	712/23
27	US 5745721 A	☒	Partitioned addressing apparatus for vector/scalar registers	712/208
28	US 5729726 A	☒	Method and system for performance monitoring efficiency of branch unit operation in a processing system	712/233
29	US 5726823 A	☒	Method of detecting positioning of a magnetic head, and a magnetic disk device	360/77.08
30	US 5717881 A	☒	Data processing system for processing one and two parcel instructions	712/205
31	US 5706490 A	☒	Method of processing conditional branch instructions in scalar/vector processor	712/234
32	US 5696946 A	☒	Method and apparatus for efficient transfer of data to memory	345/559
33	US 5691920 A	☒	Method and system for performance monitoring of dispatch unit efficiency in a processing system	702/186
34	US 5680572 A	☒	Cache memory system having data and tag arrays and multi-purpose buffer assembly with multiple line buffers	711/126
35	US 5671444 A	☒	Methods and apparatus for caching data in a non-blocking manner using a plurality of fill buffers	710/52
36	US 5671439 A	☒	Multi-drive virtual mass storage device and method of operating same	710/1
37	US 5659706 A	☒	Vector/scalar processor with simultaneous processing and instruction cache filling	711/125
38	US 5649173 A	☒	Hardware architecture for image generation and manipulation	345/501
39	US 5640524 A	☒	Method and apparatus for chaining vector instructions	712/222
40	US 5623650 A	☒	Method of processing a sequence of conditional vector IF statements	712/234
41	US 5606707 A	☒	Real-time image processor	345/418
42	US 5598547 A	☒	Vector processor having functional unit paths of differing pipeline lengths	712/222
43	US 5577200 A	☒	Method and apparatus for loading and storing misaligned data on an out-of-order execution computer system	714/50

	Document ID	U	Title	Current OR
1	US 20020016906 A1	☐	Instruction fetch unit aligner	
2	US 20020010793 A1	☒	METHOD AND APPARATUS FOR PERFORMING FRAME PROCESSING FOR A NETWORK	
3	US 20010052065 A1	☒	EFFICIENT SAVING AND RESTORING STATE IN TASK SWITCHING	
4	US 20010037434 A1	☒	Store to load forwarding using a dependency link file	
5	US 6321325 B1	☒	Dual in-line buffers for an instruction fetch unit	712/204
6	US 6314509 B1	☒	Efficient method for fetching instructions having a non-power of two size	712/204
7	US 6297857 B1	☒	Method for accessing banks of DRAM	348/714
8	US 6285825 B1	☒	Optical disc, recording apparatus, a computer-readable storage medium storing a recording program, and a recording method	386/98
9	US 6266744 B1	☒	Store to load forwarding using a dependency link file	711/146
10	US 6253300 B1	☒	Computer partition manipulation during imaging	711/173
11	US 6249861 B1	☒	Instruction fetch unit aligner for a non-power of two size VLIW instruction	712/204
12	US 6175472 B1	☒	Method for generating a position error signal calibration curve in a hard disk drive	360/135
13	US 6161208 A	☒	Storage subsystem including an error correcting cache and means for performing memory to memory transfers	714/764
14	US 6141747 A	☒	System for store to load forwarding of individual bytes from separate store buffer entries to form a single load word	712/225
15	US 6125435 A	☒	Alignment of cluster address to block addresses within a semiconductor non-volatile mass storage memory	711/201
16	US 6125232 A	☒	Large-capacity recording medium, method and apparatus for reproducing data from a large capacity recording medium, and method and apparatus for recording data on a large-capacity recording medium	386/95
17	US 6112297 A	☒	Apparatus and method for processing misaligned load instructions in a processor supporting out of order execution	712/225
18	US 5949971 A	☒	Method and system for performance monitoring through identification of frequency and length of time of execution of serialization instructions in a processing system	714/47
19	US 5909567 A	☒	Apparatus and method for native mode processing in a RISC-based CISC processor	712/208
20	US 5797019 A	☒	Method and system for performance monitoring time lengths of disabled interrupts in a processing system	710/262
21	US 5793378 A	☒	Implementation for high speed arbitrary angle of rotation	345/649

	Document ID	U	Title	Current OR
22	US 5499380 A	☒	Data processor and read control circuit, write control circuit therefor	711/212
23	US 5463748 A	☒	Instruction buffer for aligning instruction sets using boundary detection	712/204
24	US 5400369 A	☒	Fram aligner with reduced circuit scale	375/368
25	US 5351047 A	☒	Data decoding method and apparatus	341/67
26	US 5307504 A	☒	System and method for preserving instruction granularity when translating program code from a computer having a first architecture to a computer having a second reduced architecture during the occurrence of interrupts due to asynchronous events	712/41
27	US 5170477 A	☒	Odd boundary address aligned direct memory acess device and method	711/201
28	US 5081654 A	☒	Parallel bit detection circuit for detecting frame synchronization information imbedded within a serial bit stream and method for carrying out same	375/368
29	US 5073891 A	☒	Method and apparatus for testing memory	714/720
30	US 5058140 A	☒	Self-correcting serial baud/bit alignment	375/360
31	US 4879731 A	☒	Apparatus and method for sync detection in digital data	375/368
32	US 4814976 A	☒	RISC computer with unaligned reference handling and method for the same	711/201
33	US 4740941 A	☒	System for aligning sector marks with data in a disk storage system	369/47.31
34	US 4675830 A	☒	Method for producing a scaleable typeface data	345/666
35	US 4390912 A	☒	Transducer positioning system and data disk therefor	360/78.14
36	US 4131763 A	☒	Bit switching of word synchronized data	370/368
37	US 4050811 A	☒	Optical data record copier having array of lenses with field gaps aligned with data gaps	355/46

	Document ID	U	Title	Current OR
1	US 6349383 B1	☐	System for combining adjacent push/pop stack program instructions into single double push/pop stack microinstuction for execution	712/226
2	US 6208772 B1	☒	Data processing system for logically adjacent data samples such as image data in a machine vision system	382/308
3	US 6157971 A	☒	Source-destination re-timed cooperative communication bus	710/100
4	US 6011788 A	☒	S-CDMA fixed wireless loop system employing subscriber unit/radio base unit super-frame alignment	370/335
5	US 6000018 A	☒	System for aligning control words for identifying boundaries of headerless data sectors using automatic incrementing and discarding of data frame numbers	711/154
6	US 5983305 A	☒	Network adapter with data aligner	709/250
7	US 5912673 A	☒	Graphical image convolution using multiple pipelines	345/643
8	US 5896140 A	☒	Method and apparatus for simultaneously displaying graphics and video data on a computer display	345/536
9	US 5889997 A	☒	Assembler system and method for a geometry accelerator	717/151
10	US 5870578 A	☒	Workload balancing in a microprocessor for reduced instruction dispatch stalling	712/215
11	US 5822559 A	☒	Apparatus and method for aligning variable byte-length instructions to a plurality of issue positions	712/214
12	US 5751981 A	☒	High performance superscalar microprocessor including a speculative instruction queue for byte-aligning CISC instructions stored in a variable byte-length format	712/204
13	US 5748978 A	☒	Byte queue divided into multiple subqueues for optimizing instruction selection logic	712/23
14	US 5729727 A	☒	Pipelined processor which reduces branch instruction interlocks by compensating for misaligned branch instructions	712/233
15	US 5721841 A	☒	Adapter having data aligner including register being loaded to or from memory with an offset in accordance with predetermined network fragmentation parameters	710/316
16	US 5675617 A	☒	Synchronous protocol encoding and decoding method	375/365
17	US 5644744 A	☒	Superscaler instruction pipeline having boundary identification logic for variable length instructions	712/207
18	US 5640526 A	☒	Superscaler instruction pipeline having boundary indentification logic for variable length instructions	712/207
19	US 5617549 A	☒	System and method for selecting and buffering even and odd instructions for simultaneous execution in a computer	712/206
20	US 5586277 A	☒	Method for parallel steering of fixed length fields containing a variable length instruction from an instruction buffer to parallel decoders	712/210
21	US 5524265 A	☒	Architecture of transfer processor	712/38

	Document ID	U	Title	Current OR
47	US 4466150 A	☒	Toothbrush	15/143.1
48	US 4407439 A	☒	Apparatus for depositing a web of material on a table	226/20
49	US 4281385 A	☒	Control system for a machine tool	700/192
50	US 4208679 A	☒	Transducer positioning system for rotating disk drive units	360/77.08
51	US 4135242 A	☒	Method and processor having bit-addressable scratch pad memory	712/245
52	US 4005490 A	☒	Magnetic disc memory	360/99.08
53	US 3972068 A	☒	System for translating magnetically encoded data to visually readable characters corresponding thereto	360/4
54	US 3889593 A	☒	Electric-set numbering wheel	101/110
55	US 3783778 A	☒	DATA INDICATING DEVICE FOR PRINTING MACHINES	101/45
56	US 3783522 A	☒	METHOD AND APPARATUS FOR SHAFT ALIGNMENT	33/661
57	US 3770903 A	☒	IMAGE DATA RATE CONVERTER HAVING A DRUM WITH A FIXED HEAD AND A ROTATABLE HEAD	360/8
58	US 3770265 A	☒	CARD FEEDER	271/10.06

	Document ID	U	Title	Current OR
1	US 6330623 B1	☐	System and method for maximizing DMA transfers of arbitrarily aligned data	710/23
2	US 6320718 B1	☒	Disk drive with zero read offset in reserved area and method of making same	360/77.04
3	US 6266453 B1	☒	Automated image fusion/alignment system and method	382/294
4	US 6236536 B1	☒	System and method of servo compensation for friction induced off track problem in a data storage device	360/99.08
5	US 6152803 A	☒	Substrate dicing method	451/12
6	US 6088386 A	☒	Transmitter with phase rotor, modulator/demodulator, communication system and method performed thereby	375/222
7	US 6038050 A	☒	Rotating laser scanner head with target mounted therein and system and method for use therewith	359/196
8	US 6037733 A	☒	Robot having multiple degrees of freedom	318/568.11
9	US 5999356 A	☒	Data cartridge library with rotating storage stacks	360/71
10	US 5929330 A	☒	Visual tire cap pressure indicator	73/146.8
11	US 5922066 A	☒	Multifunction data aligner in wide data width processor	712/204
12	US 5822555 A	☒	Method and apparatus for aligning an instruction boundary in variable length macroinstructions with an instruction buffer	712/204
13	US 5802556 A	☒	Method and apparatus for correcting misaligned instruction data	711/109
14	US 5802246 A	☒	Data recording method	386/105
15	US 5789890 A	☒	Robot having multiple degrees of freedom	318/567
16	US 5774697 A	☒	Data realignment method and apparatus	711/141
17	US 5774196 A	☒	Method and apparatus of aligning color modulation data to color wheel filter segments	348/743
18	US 5729090 A	☒	Method of making an arcuate scan tape drive	29/603.18
19	US 5716141 A	☒	Precision self-contained hydrodynamic bearing assembly	384/114
20	US 5680642 A	☒	Method and apparatus for pseudo-aligned transfers of data to memory wherein a re-alignment is performed based on the data byte control header	710/33
21	US 5631889 A	☒	Optical storage apparatus with a focused mass storage medium	369/114
22	US 5625190 A	☒	Forward projection algorithm	250/363.03
23	US 5610875 A	☒	3-D converted shear wave rotation with layer stripping	367/75

	Document ID	U	Title	Current OR
24	US 5600806 A	☒	Method and apparatus for aligning an instruction boundary in variable length macroinstructions with an instruction buffer	712/204
25	US 5585978 A	☒	Arcuate scan tape drive	360/85
26	US 5579579 A	☒	Method for making precision self-contained hydrodynamic bearing assembly	29/898
27	US 5409443 A	☒	Tube holder arrangement for blood centrifuge	494/10
28	US 5402270 A	☒	Method of duplicating data on a magnetic disk with reduced duplication time	360/15
29	US 5355146 A	☒	Multi-directional hand scanner and mouse	345/156
30	US 5336030 A	☒	Buffered access system for an automated computer media storage library	414/277
31	US 5263261 A	☒	Shaft alignment data acquisition	33/645
32	US 5193036 A	☒	Transducer head skew arrangement for disk drive system	360/78.14
33	US 5149951 A	☒	Apparatus and method for presenting a data card for data transfer with centrifugal flyweight	235/485
34	US 5119254 A	☒	Data transducer position control system for rotating disk data storage equipment	360/264.7
35	US 5085623 A	☒	Bar scoring apparatus	493/400
36	US 5014875 A	☒	Medication dispenser station	221/2
37	US 4912312 A	☒	Optical card duplicating system	235/487
38	US 4860272 A	☒	Erroneous track jump restoration apparatus for optical record disc player	369/53.28
39	US 4845373 A	☒	Automatic alignment apparatus having low and high resolution optics for coarse and fine adjusting	250/548
40	US 4827422 A	☒	Fan scan horizon sensor for a spin stabilized satellite	701/226
41	US 4820913 A	☒	Multiple card recording system	235/487
42	US 4814909 A	☒	Data transducer position control system for rotating disk data storage equipment	360/78.07
43	US 4692603 A	☒	Optical reader for printed bit-encoded data and method of reading same	235/454
44	US 4575775 A	☒	Magnetic recording disk having a sector servo pattern for use with a multiple element head	360/77.08
45	US 4544242 A	☒	Optical deflecting device	359/211
46	US 4472144 A	☒	Celestial compass having rotatable means for organizing two distinct sets of astrological data	434/106

	Document ID	U	Title	Current OR
23	US 5321823 A	☒	Digital processor with bit mask for counting registers for fast register saves	712/224
24	US 5317720 A	☒	Processor system with writeback cache using writeback and non writeback transactions stored in separate queues	711/143
25	US 5287467 A	☒	Pipeline for removing and concurrently executing two or more branch instructions in synchronization with other instructions executing in the execution unit	712/235
26	US 5155843 A	☒	Error transition mode for multi-processor system	714/5
27	US 5023828 A	☒	Microinstruction addressing in high-speed CPU	712/245
28	US 5019967 A	☒	Pipeline bubble compression in a computer system	712/219
29	US 5006980 A	☒	Pipelined digital CPU with deadlock resolution	712/219
30	US 4916654 A	☒	Method for transfer of data via a window buffer from a bit-planar memory to a selected position in a target memory	345/537
31	US 4875160 A	☒	Method for implementing synchronous pipeline exception recovery	712/228
32	US 4694405 A	☒	Laser printer controller data alignment device	358/1.11

	Document ID	U	Title	Current OR
1	US 6240508 B1	☐	Decode and execution synchronized pipeline processing using decode generated memory read queue with stop entry to allow execution generated memory read	712/219
2	US 6185633 B1	☒	DMA configurable receive channel with memory width N and with steering logic compressing N multiplexors	710/22
3	US 6138206 A	☒	Data register for multicycle data cache read	711/118
4	US 6115795 A	☒	Method and apparatus for configurable multiple level cache with coherency in a multiprocessor system	711/141
5	US 6065101 A	☒	Pipelined snooping of multiple L1 cache lines	711/140
6	US 6065070 A	☒	DMA configurable channel with memory width N and with steering logic comprising N multiplexors, each multiplexor having a single one-byte input and N one-byte outputs	710/22
7	US 6049860 A	☒	Pipelined floating point stores	712/25
8	US 6032250 A	☒	Method and apparatus for identifying instruction boundaries	712/210
9	US 5940877 A	☒	Cache address generation with and without carry-in	711/220
10	US 5909694 A	☒	Multiway associative external microprocessor cache	711/128
11	US 5845100 A	☒	Dual instruction buffers with a bypass bus and rotator for a decoder of multiple instructions of variable length	712/204
12	US 5822555 A	☒	Method and apparatus for aligning an instruction boundary in variable length macroinstructions with an instruction buffer	712/204
13	US 5809320 A	☒	High-performance multi-processor having floating point unit	712/34
14	US 5758116 A	☒	Instruction length decoder for generating output length indicia to identity boundaries between variable length instructions	712/210
15	US 5608885 A	☒	Method for handling instructions from a branch prior to instruction decoding in a computer which executes variable-length instructions	712/204
16	US 5600806 A	☒	Method and apparatus for aligning an instruction boundary in variable length macroinstructions with an instruction buffer	712/204
17	US 5590293 A	☒	Dynamic microbranching with programmable hold on condition, to programmable dynamic microbranching delay minimization	712/234
18	US 5542058 A	☒	Pipelined computer with operand context queue to simplify context-dependent execution flow	713/502
19	US 5481689 A	☒	Conversion of internal processor register commands to I/O space addresses	711/202
20	US 5471628 A	☒	Multi-function permutation switch for rotating and manipulating an order of bits of an input data byte in either cyclic or non-cyclic mode	712/223
21	US 5394529 A	☒	Branch prediction unit for high-performance processor	712/240
22	US 5333296 A	☒	Combined queue for invalidates and return data in multiprocessor system	711/171

	L #	Hits	Search Text	DBs
1	L1	11565	(misalign$3 align$3) near10 (data operand instruction)	USPAT; US-PGPUB
2	L2	11620	(misalign$3 align$3 unalign$3) near10 (data operand instruction)	USPAT; US-PGPUB
3	L3	1027	2 near20 boundary	USPAT; US-PGPUB
4	L4	343	3 near50 (memory load$3 stor$3)	USPAT; US-PGPUB
5	L6	94	4 and rotat$3	USPAT; US-PGPUB
6	L7	837	((misalign$3 align$3) near10 (data operand instruction)).ab,ti.	USPAT; US-PGPUB
7	L8	843	((misalign$3 align$3 unalign$3) near10 (data operand instruction)).ab,ti.	USPAT; US-PGPUB
8	L12	249	4 not (5 6 9 10 11)	USPAT; US-PGPUB
9	L5	32	3 near99 rotat$3	USPAT; US-PGPUB
10	L9	58	8 and rotat$3.ab,ti.	USPAT; US-PGPUB
11	L10	37	3 and 8 not (4 5 6 9)	USPAT; US-PGPUB
12	L11	65	6 not (9 5)	USPAT; US-PGPUB